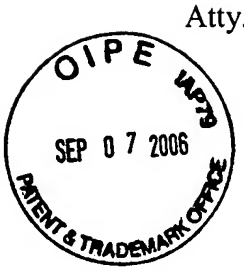
Atty. Docket No.: 24295/81003



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Adrian E. Ong
Title:	Chip Testing Within a Multi-Chip Semiconductor Package
Application No.:	10/824,734
Filing Date:	April 15, 2004
Examiner:	Dipakkumar B. Gandhi
Group Art Unit:	2138
Confirmation No.:	6737
Law Office:	Sidley Austin LLP

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Examiner Gandhi:

Applicant submits six (6) sheets of formal drawings, consisting of Figures 1, 2, 3, 4, 5, 6, 7, 8, 9, and 10, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (415) 772-7428.

EXPRESS MAIL LABEL NO.:

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Respectfully submitted,

By: _____

Philip W. Woo
Attorney of Record
Registration No. 39,880
PWW/rp

September 7, 2006

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